Faculty of Computers and Artificial Intelligence

CS221: Logic Design

## Assignment no 05: Chapter 6

Note: You can check the exercises after the book Chapter. In our assignment, we are using the 11th edition of "Digital Fundamentals" By Thomas L. Floyd"

Section 6–2 Parallel Binary Adders

4. For the parallel adder in Figure 6–69, **determine** the complete sum by analysis of the logical operation of the circuit. **Verify** your result by longhand addition of the two input numbers.
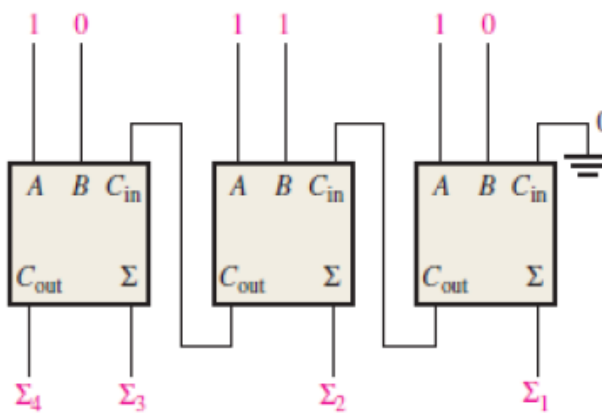
FIGURE 6–69

6. The circuit shown in Figure 6–71 is a 4-bit circuit that can add or subtract numbers in a form used in computers (positive numbers in true form; negative numbers in complement form). (a)**Explain** what happens when the Add/Sub. input is HIGH. (b) **What** happens when Add/Sub. is LOW?
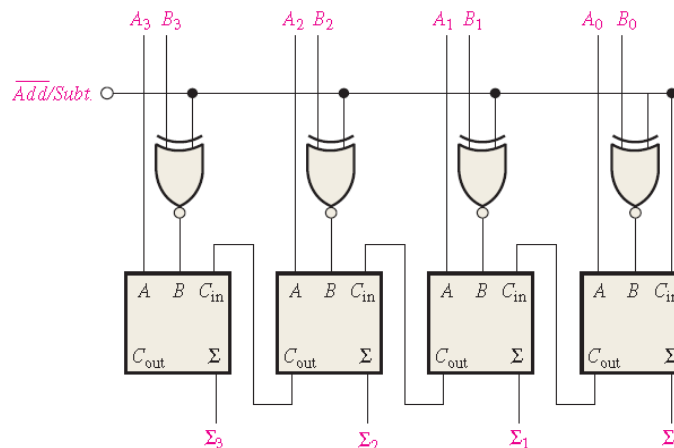
FIGURE 6–71

8. The input waveforms in Figure 6–72 is applied to a 2-bit adder. **Determine** the waveforms for the sum and the output carry in relation to the inputs by constructing a timing diagram.
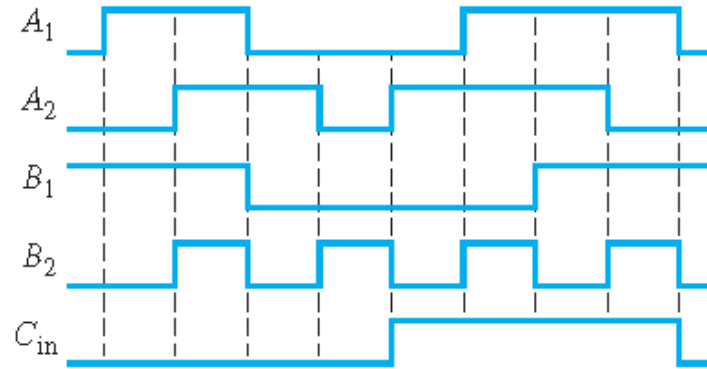

FIGURE 6–72

14. For the 4-bit comparator in Figure 6–74, **plot** each output waveform for the inputs shown. The outputs are active-HIGH.
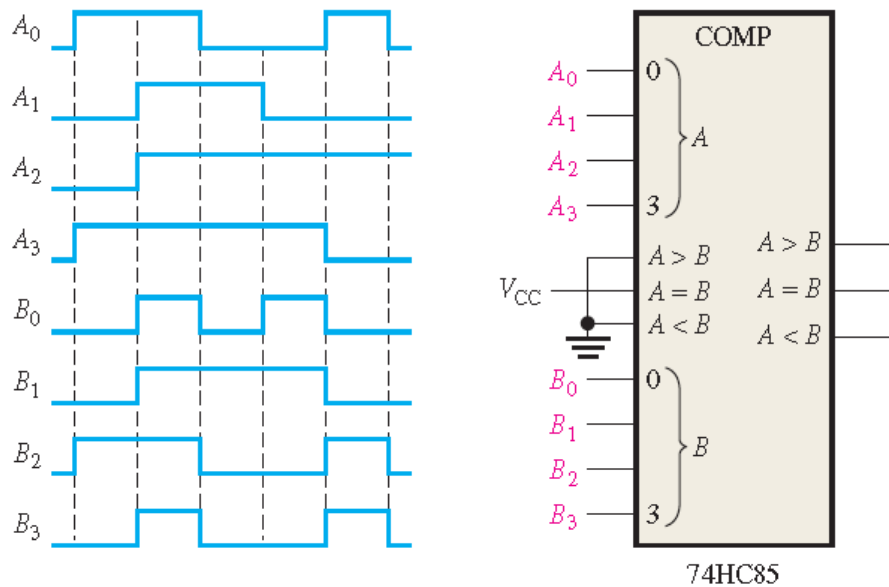

FIGURE 6–74

16. When a LOW is on the output of each of the decoding gates in Figure 6–75, **what** is the binary code appearing on the inputs? The MSB is A3.
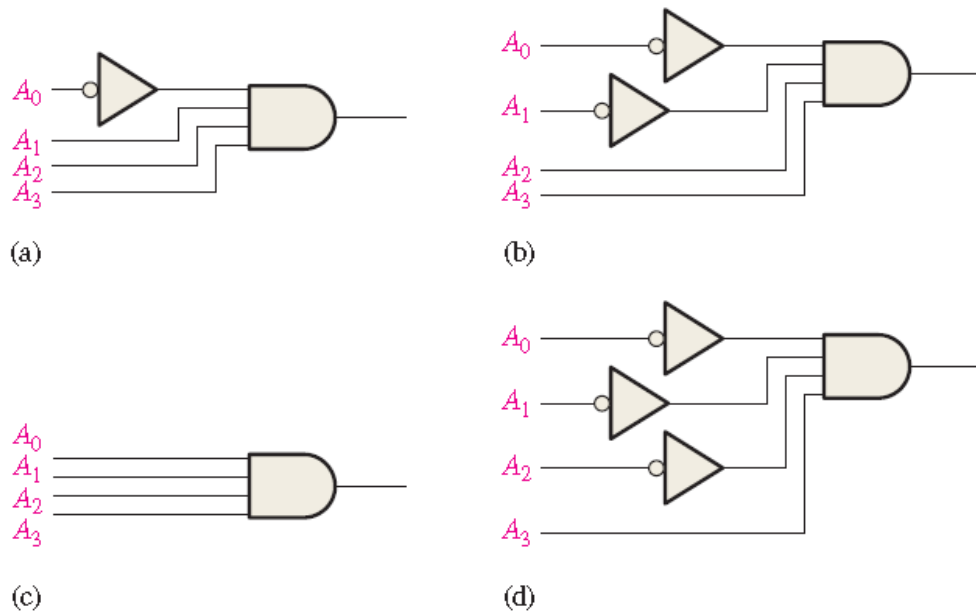

(a)

(b)

(c)

(d)

FIGURE 6–75

20. If the input waveforms are applied to the decoding logic as indicated in Figure 6–76, **sketch** the output waveform in proper relation to the inputs.
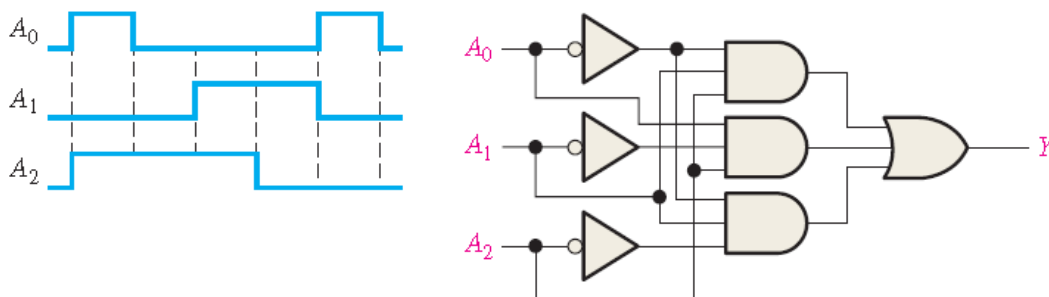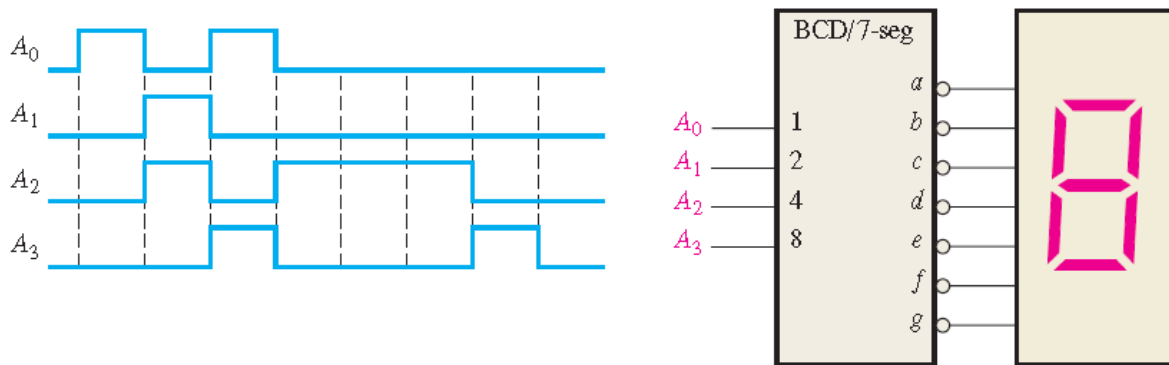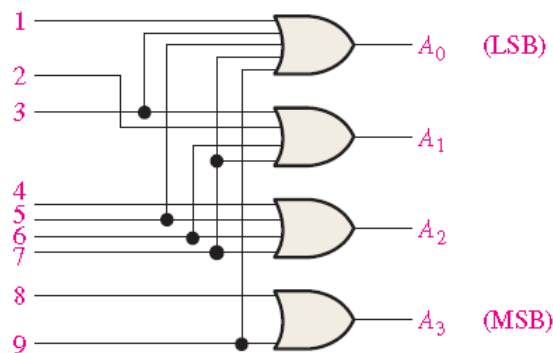

FIGURE 6–76

22. A 7-segment decoder/driver drives the display in Figure 6–78. If the waveforms are applied as indicated, **determine** the sequence of digits that appears on the display.

FIGURE 6–78

23. For the decimal-to-BCD encoder logic of Figure 6–37, assume that the 9 input and the 3 input are both HIGH. **What** is the output code? **Is** it a valid BCD (8421) code?

FIGURE 6–37 Basic logic diagram of a decimal-to-BCD encoder. A 0-digit input is not needed because the BCD outputs are all LOW when there are no HIGH inputs.

26. **Show** the logic required to convert a 10-bit binary number to Gray code and use that logic to convert the following binary numbers to Gray code:

(a) 1010111100   (b) 1111000011   (c) 1011110011   (d) 1000000001

28. For the multiplexer in Figure 6–79, **determine** the output for the following input states: D0 = 1, D1 = 0, D2 = 0, D3 = 1, S0 = 0, S1 = 1.
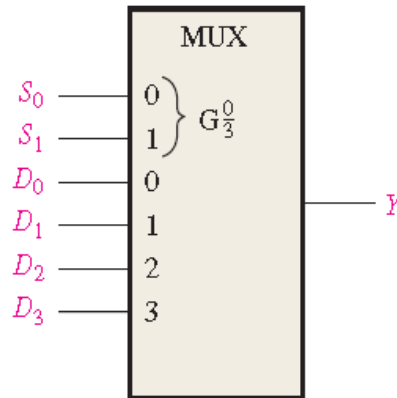

FIGURE 6–79

29. If the data-select inputs to the multiplexer in Figure 6–79 are sequenced as shown by the waveforms in Figure 6–80, **determine** the output waveform with the data inputs specified in Problem 28.
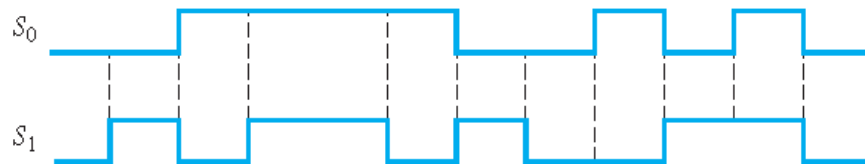

FIGURE 6–80

32. The waveforms in Figure 6–82 is applied to the 4-bit parity logic. **Determine** the output waveform in proper relation to the inputs. For how many bit times does even parity occur, and **how** is it indicated? The timing diagram includes eight-bit times.
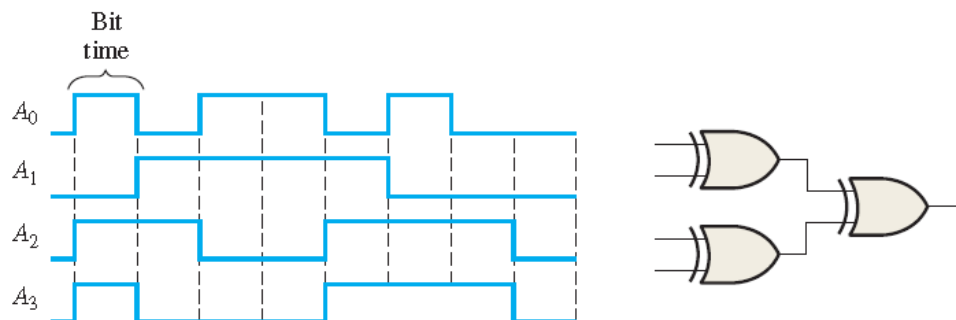

FIGURE 6–82